Remarks & Arguments

In the Office Action, the Examiner noted that Claims 12-26 are pending in the application, and that Claims 12-26 are rejected. By this amendment, Claims 12, 13, 16-19 and 21-23 have been amended and Claims 27-29 have been added. Thus, Claims 12-29 are pending in the application. The amendments to the claims do not add new matter to the application. The Examiner's rejections are traversed below.

Rejections Under 35 U.S.C. 102

Claims 12-26 stand rejected under 35 U.S.C. 102 as being anticipated by U.S. Patent Application Publication No. 2002/0156998 to Casselman. Applicant respectfully traverses the rejection of Claims 12-26 on the basis that the relied upon reference does not disclose every element in the independent Claim 12, 16 19 and 23 as amended.

In particular, Claim 12 as amended recites a method comprising "establishing an interface between a host computer and a general purpose programmable hardware device; transmitting configuration information over said interface in a first transmission mode to configure the general purpose programmable hardware device **to function** according to a programmed configuration **as virtual device under test**; and transmitting **operation information from said virtual device under test emulating operation of an actual device under tests** and **operation information from said actual device under test** over said interface in a second transmission mode." In contrast, Casselman discloses a technique that includes 1)

"at least one of the FPGAs in at least one of the distributed virtual computers is automatically configured ... into a microprocessor-like device which then" 2) "configures one or some "control" FPGAs or "control" portions of single FPGAs in the various distributed virtual computers to give them control or "compiling" capability over the remaining FPGA resources, which" 3) "act as a computation FPGA array." Thus, Casselman does not disclose configuring a general purpose programmable hardware device to function as a virtual device under test. In addition, Casselman does not disclose that the virtual device under test emulates operation of an actual device under tests. Casselman also does not disclose transmitting operation information from the virtual device under test emulating the actual device under test and the actual device under test. Furthermore, Casselman does not disclose that the virtual device under test is configured over an interface in a first transmission mode and that the operation information from both the virtual device under test and the actual device under test are transmitted over the same interface in a second transmission mode.

For each of the reasons set forth above, Applicant respectfully submits that Claim 12 is patentable over Casselman. Accordingly, Applicant requests that the anticipation rejection of Claim 12 be withdrawn and that Claim 12 be allowed. In addition, **Claims 13-15** are allowable by virtue of their dependency on respective base Claim 12, as well as the additional elements they recite. Accordingly, Applicant also respectfully requests that the anticipation rejection of Claims 13-15 be withdrawn and that Claims 13-15 be allowed.

Claim 16 as amended recites a method comprising "communicating configuration information between a host computer and a virtual device under test (DUT) to configure the

virtual DUT to **emulate** a DUT; executing instructions in **synchronization** on the DUT and the virtual DUT; and transmitting operation information, from said executing by the DUT and the virtual DUT, between the host computer and the virtual DUT." In contrast, Casselman discloses a technique that includes 1) "at least one of the FPGAs in at least one of the distributed virtual computers is automatically configured ... into a microprocessor-like device which then" 2) "configures one or some "control" FPGAs or "control" portions of single FPGAs in the various distributed virtual computers to give them control or "compiling" capability over the remaining FPGA resources, which" 3) "act as a computation FPGA array." Thus, Casselman does not disclose any of the limitations of Claim 16 as amended. Thus, the technique disclosed in Casselman does not involve a virtual DUT emulating a DUT, or the DUT and virtual DUT executing instructions in synchronization.

Applicant therefore respectfully submits that Claim 16 is patentable over Casselman. Accordingly, Applicant requests that the anticipation rejection of Claim 16 be withdrawn and that Claim 16 be allowed. In addition, **Claims 17 and 18** are allowable by virtue of their dependency on respective base Claim 16, as well as the additional elements they recite. Accordingly, Applicant also respectfully requests that the anticipation rejection of Claims 17 and 18 be withdrawn and that Claims 17 and 18 be allowed.

Claim 19 as amended recites a method comprising "connecting a host computer to a base station using a communication interface, wherein the base station includes a field programmable gate array (FPGA); programming an emulator configuration into the FPGA using the communication interface; and receiving operation information from a device under test (DUT)

and the FPGA emulating the DUT using the communication interface." In contrast, Casselman discloses a technique that includes 1) "at least one of the FPGAs in at least one of the distributed virtual computers is automatically configured ... into a microprocessor-like device which then" 2) "configures one or some "control" FPGAs or "control" portions of single FPGAs in the various distributed virtual computers to give them control or "compiling" capability over the remaining FPGA resources, which" 3) "act as a computation FPGA array." Thus, Casselman does not disclose programming an emulator configuration into an FPGA. Casselman also does not disclose receiving operation information from the DUT and the FPGA emulating the DUT.

For each of the reasons set forth above, Applicant respectfully submits that Claim 19 is patentable over Casselman. Accordingly, Applicant requests that the anticipation rejection of Claim 19 be withdrawn and that Claim 19 be allowed. In addition, **Claims 20-22** are allowable by virtue of their dependency on respective base Claim 19, as well as the additional elements they recite. Accordingly, Applicant also respectfully requests that the anticipation rejection of Claims 20-22 be withdrawn and that Claims 220-22 be allowed.

Claim 23 as amended recites a method comprising "transmitting interface information over a parallel communication interface of a field programmable gate array (FPGA) to configure the FPGA to act as a parallel port; transmitting **emulator** information to the FPGA to configure the FPGA to operate as a virtual microcontroller **in lock step** with a microcontroller under test using the parallel port of the FPGA; and receiving operation information, generated by the virtual microcontroller and the microcontroller under test operating in lock step, from the parallel port of the FPGA." In contrast, Casselman discloses a technique that includes 1) "at least one of

the FPGAs in at least one of the distributed virtual computers is automatically configured ... into a microprocessor-like device which then" 2) "configures one or some "control" FPGAs or "control" portions of single FPGAs in the various distributed virtual computers to give them control or "compiling" capability over the remaining FPGA resources, which" 3) "act as a computation FPGA array." Thus, Casselman does not disclose transmitting emulator information to the FPGA to operate as a virtual microcontroller. In addition, Casselman does not disclose that the configured virtual microcontroller is configured to operate in lock step with the microcontroller under test. Casselman also does not disclose receiving operation information, generated by the virtual microcontroller and the microcontroller under test operating in lock step. Furthermore, Casselman does not disclose that the FPGA is also configured to act as a parallel port and that the operation information from both the virtual microcontroller and the microcontroller under test are received from the configured parallel port of the FPGA.

For each of the reasons set forth above, Applicant respectfully submits that Claim 23 is patentable over Casselman. Accordingly, Applicant requests that the anticipation rejection of Claim 23 be withdrawn and that Claim 23 be allowed. In addition, **Claims 24-26** are allowable by virtue of their dependency on respective base Claim 23, as well as the additional elements they recite. Accordingly, Applicant also respectfully requests that the anticipation rejection of Claims 24-26 be withdrawn and that Claims 24-26 be allowed.

Conclusion

For all the reasons advanced above, Applicant respectfully submits that the present application is in condition for allowance and that action is earnestly solicited. The Examiner is invited to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

The Commissioner is hereby authorized to charge any additional fees, which may be required for this amendment, or credit any overpayment, to Deposit Account 23-0085. In the event that an extension of time is required, or may be required in addition to that requested in a petition for an extension of time, the Commissioner is requested to grant a petition for that extension of time which is required to make this response timely and is hereby authorized to charge any fee for such an extension of time or credit any overpayment for an extension of time to Deposit Account 23-0085.

Respectfully submitted,

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